REMARKS

Reconsideration of this application as amended is respectfully requested.

In the Office Action, claims 1, 3-8, 11-16, and 18-22 were pending and rejected. In this response, no claim has been canceled. Claims 1, 3-8, 11-16, and 18-22 have been amended. In addition, new claims 28-36 have been added. Thus, claims 1, 3-8, 11-16, 18-22, and 28-36 remain pending. No new matter has been added.

Claims 1 and 3-7 are rejected under 35 U.S.C. 112, first paragraph. In view of the foregoing amendments, the rejections have been overcome. It is respectfully submitted that the support for claims 1 and 3-7 can be found on page 16 of the specification.

Claims 1, 3, 8, 15-16, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,216,718 of Stracovsky et al. ("Stracovsky") in view of U.S. published patent application 2002/012,921 of Yoo ("Yoo"). Claims 4-7, 11-14, and 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky in view of Yoo and U.S. Patent No. 6,381,671 of Ayukawa et al. ("Ayukawa").

Although Yoo claims a benefit of a provisional application that was filed before the filing date of the present application, the filing date of Yoo is after the filing date of the present application. Therefore, only the disclosure of the provisional may be used against the present application.

It is respectfully submitted that the currently pending claims of the present application include limitations that are not disclosed by the cited references, individually or in combination. Specifically, independent claim 1 as amend recites as follows:

1. An apparatus, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache located on a memory module via a plurality of command lines and address lines over a memory bus, the command sequencer and serializer unit to cause a current line of data to be read out of a memory module memory device and to load a next line of data from the memory module memory device to the data cache, in response to a single command having a plurality of segments serialized and sequentially transmitted via the plurality of address lines and command lines over the memory bus within a memory access transaction.

(Emphasis added)

Independent claim 1 includes limitations that, in response to a single command (e.g., a read and preload command) having multiple segments and serialized and sequentially transmitted over multiple command and address lines within a single memory access transaction, a current line of data being accessed is read out from a memory module. In addition, a next line of data is also read out from the memory module and stored in the data cache because it is most likely that a next memory access may be addressed to the next line of data. It is respectfully submitted that none of the cited references, individually or in combination, discloses or suggests the above limitations.

Rather, Stracovsky and Yoo merely disclose a conventional memory controller. Although Ayukawa discloses an address/command self-prefetching unit (see, col. 12, lines 12-18), Ayukawa still fails to disclose or suggest that a single command having multiple segments that are serialized and sequentially transmitted to cause a current line of data being read from the memory and an additional line of data being read and stored in the cache. There is no mention of a single command having multiple segments with each segment being transmitted via one of the command and address lines within one of the multiple transfer periods in Ayukawa, particularly, according to the formats recited in claims 28-36.

It is respectfully submitted that the cited references, individually or in combination, fail to disclose or suggest the limitations set forth above. Therefore, for the reasons discussed above, it is respectfully submitted that independent claim 1 is patentable over the cited references.

Similarly, independent claims 8 and 15 include limitations similar to those recited in claim 1. Thus, for the reasons similar to those discussed above, independent claims 8 and 15 are patentable over the cited references.

Given that the rest of the claims depend from one of the above independent claims, at least for the reasons similar to those discussed above, it is respectfully submitted that the rest of the claims are patentable over the cited references. Withdrawal of the rejections is respectfully requested.

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

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